CLAIMS:

1. A system comprising:

a shared memory; and

a plurality of processing elements coupled to said shared memory, wherein each of said plurality of processing elements comprises a processing unit, a direct memory access controller and a plurality of attached processing units, wherein said direct memory access controller comprises an address translation mechanism, wherein each of said plurality of attached processing units is configured to access said shared memory in a restricted manner.

2. The system as recited in claim 1, wherein each of said plurality of attached processing units is configured to issue a request to an associated direct memory access controller to access said shared memory, wherein said request specifies a range of addresses to be accessed as virtual addresses.

3. The system as recited in claim 2, wherein said associated direct memory access controller is configured to translate said range of virtual addresses to be accessed.

4. The system as recited in claim 3, wherein said associated direct memory access controller translates said range of virtual addresses to be accessed by retrieving an associated range of physical addresses from said address translation mechanism.

5. The system as recited in claim 3, wherein said associated direct memory access controller translates said range of virtual addresses to be accessed by retrieving an associated range of physical addresses from a page table in said shared memory.

6. The system as recited in claim 1, wherein said address translation mechanism is a translation lookaside buffer.

7. The system as recited in claim 4, wherein said associated direct memory access controller comprises a manager, wherein said manager is configured to search said address translation mechanism for said associated range of physical addresses.

8. The system as recited in claim 5, wherein said associated direct memory access controller comprises a manager, wherein said manager is configured to search said page table in said shared memory for said associated range of physical addresses.

9. The system as recited in claim 3, wherein said range of virtual addresses to be accessed are translated into an associated range of physical addresses, wherein said associated range of physical addresses are pinned.

10. A method for attached processing units accessing a shared memory in a system comprising the steps of:

issuing a request to an associated direct memory access controller to access said shared memory, wherein said request specifies a range of addresses to be accessed as virtual addresses; and

translating said range of virtual addresses to be accessed to an associated range of physical addresses by said associated direct memory access controller.

11. The method as recited in claim 10, wherein said associated direct memory access controller translates said range of virtual addresses to be accessed by retrieving said associated range of physical addresses from an address translation mechanism.

12. The method as recited in claim 10, wherein said associated direct memory access controller translates said range of virtual addresses to be accessed by retrieving said associated range of physical addresses from a page table in said shared memory.

13. The method as recited in claim 11, wherein said address translation mechanism is a translation lookaside buffer.

14. The method as recited in claim 10, wherein said associated range of physical addresses are pinned.

15. A method for maintaining Translation Lookaside Buffer (TLB) consistency in a system comprising a shared memory and a plurality of processing elements coupled to said shared memory, wherein each of said plurality of processing elements comprises a processing unit, a direct memory access controller and a plurality of attached processing units, wherein each of said plurality of direct memory access controllers comprises a TLB, the method comprising the steps of:

invalidating a copy of a page table entry that was updated in a particular TLB of a direct memory access controller associated with a particular processing unit by said particular processing unit;

broadcasting a TLB invalided entry instruction to each of said plurality of processing units other than said particular processing unit by said particular processing unit;

determining whether to invalidate any entries in the TLB's associated with each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit; and

issuing a synchronization instruction to each of said plurality of processing units other than said particular processing unit by said particular processing unit.

16. The method as recited in claim 15, wherein each of said plurality of processing units other than said particular processing unit that received said TLB invalidated entry instruction is configured to search through the entries of said TLB's of its associated direct memory access controllers to determine whether there are any invalid entries in the TLB's associated with each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit.

17. The method as recited in claim 15, wherein each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit is configured to search through the entries of its associated TLB's to determine whether there are any invalid entries in each of said TLB's associated with each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit.

18. The method as recited in claim 16, wherein each of said plurality of processing units other than said particular processing unit invalidates any invalid entries in said TLB's of its associated direct memory access controllers.

19. The method as recited in claim 17, wherein each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit invalidates any invalid entries in its associated TLB's.

20. The method as recited in claim 15 further comprising the step of:

issuing an acknowledgment to said particular processing unit that any invalid entries were invalidated.

21. The method as recited in claim 20, wherein each of said plurality of processing units other than said particular processing unit issues an acknowledgment to said particular processing unit that any invalid entries in the TLB's associated with each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit were invalidated.

22. The method as recited in claim 20, wherein each of said plurality of direct memory access controllers other than the direct memory access controller associated with said particular processing unit issues an acknowledgment to said particular processing unit that any invalid entries in its associated TLB's were invalidated.